INFO: [VRFC 10-2263] Analyzing Verilog file "C:/Users/eacm3/Desktop/project\_3/project\_3.sim/sim\_1/impl/timing/xsim/Testbench\_full\_adder\_time\_impl.v" into library xil\_defaultlib

INFO: [VRFC 10-311] analyzing module full\_adder

INFO: [VRFC 10-311] analyzing module glbl

INFO: [VRFC 10-163] Analyzing VHDL file "C:/Users/eacm3/Desktop/project\_3/project\_3.srcs/sim\_1/imports/full adder/full\_adder\_tb.vhd" into library xil\_defaultlib

INFO: [VRFC 10-307] analyzing entity Testbench\_full\_adder